Flip-chip mounted, Ku band power amplifier compliant with space applications

O. Vendier, J-P. Fraysse, C. Schaffauser, M. Paillard, C. Drevon, J-L. Cazaux, D. Floriot[1], N. Caillas-Devignes[1], H. Blanck[2], P. Auxemery[3], W. de Ceuninck[4], R. Petersen[4], N. Haese[5], P-A. Rolland[5]

Alcatel Space - 26 av JF Champollion, BP1187
31037-TOULOUSE CEDEX 1, France
Fax : 33 5 34 35 69 47
Phone : 33 5 34 35 66 35
Email : Olivier.Vendier@space.alcatel.fr

[1] Thalès TRT-Fr -Domaine de Corbeville 91404 Orsay Cedex -France
[2] United Monolithic Semiconductors GmBH - Wilhem-Runge Strasse 11 -D-89081 ULM Germany
[3] United Monolithic Semiconductors SAS – Route Départementale 128 - 91401 Orsay Cedex- France
[4] IMOMEC, Instituut voor Materiaalonderzoek,B-3590 Diepenbeek, Belgium
[5] Institut d'Electronique et de Microélectronique du Nord - Cité Scientifique – Avenue Poincaré - BP69-59652 Villeneuve d'Ascq Cedex – France

Abstract — **Following the trends of today's increased power density into power components arena, latest developments on advanced thermal management at component level are presented. Power flip chip technology was applied to commercial HB20P heterostructure bipolar transistor technology from UMS. Results of flip-chip mounted high power amplifier on Aluminum Nitride, packaged in a space compatible micro-package are discussed.**

I. Introduction

Following the trends of today's increased power density into RF power components arena, innovative thermal management at component level is needed, especially for space application. Strong constraints on junction temperature, 115°C in most space missions, GaAs based high power density devices such as heterostructure bipolar transistor (HBT) (3.5 W/mm to be compared to 0.6-0.8 W/mm for high electron mobility transistor (HEMT)) may become unattractive. Flip-chip technology (FC) is a promising candidate for the use in a new generation of broadband multimedia satellites where thermal management and miniaturisation are key enabling criterias. Applying flip-chip technology to high power GaAs based devices (HBT) but also to GaN based devices (HEMT) have been demonstrated by several research institutes and company's over the past years with impressive results [1][2][3][4]. But none of them would assess on coefficient of thermal expansion (CTE) mismatch that occures between GaAs and dissipative susbtrate such as Aluminum Nitride (AlN) and on the means to overcome it.

In this paper, we report the latest results obtained on flip-chip mounted Ku band, HBT based, power amplifier. Flip-chip mounting was done on AlN substrate using pure gold-gold thermocompression bonding. We are focusing herein on the electrical performances of the flip-chip mounted high power amplifier (HPA) monolithic microwave integrated circuit (MMIC) into space compliant package. Assessment on the electrical impact of underfill, needed for this kind of assembly, is also given.

II. Technology Development & Fabrication

The work is based on the HB20P (power HBT up to Ku band) of United Monolithic Semiconductors which was adapted to incorporate electroplated thermal and signal bumps at wafer level. In order to reduce the stress induced into the HBT active area the thermal bump was shifted from the emitter finger together with air bridge reinforcement using high performance polymer. Details of this study are reported elsewhere [5]. The electrical impact of this polymer was implemented into the HBT

0-7803-7239-5/02/$10.00 © 2002 IEEE

extrinsic model (parasitic capacitance). Baseline configuration is depicted in Fig.1.

Fig.2 is showing a SEM picture of the 3 stages HPA MMIC after Au gold plated bumps realized on 4 inches wafers. On wafer measurements were done prior flip chip mounting on fully equipped CuW micro package. A very low loss coplanar to microstrip transition was developed in order to remain comptible with this standard micropackage. AlN subtrate together with chip capacitor were all brazed in one step using AuSn solder.

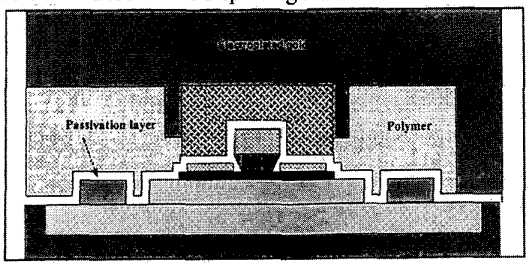

Fig.1 : Cross section of the HBTstructure at the emitter level ready to receive

A picture of the HPA, flip-chip mounted into flight model micro package is shown in Fig.3.

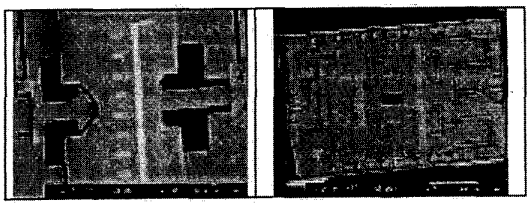

Fig.2 : Detailed SEM picture of 8 finger HBT with shifted thermal bump and overall SEM picture of the HPA after bump process.

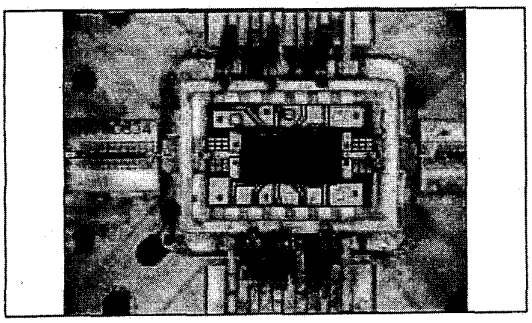

Fig.3 : Micro-photography of Flip-chip mounted HPA MMIC into its space compliant micropackage.

III. FLIP-CHIP MOUNTING EFFECTS AND ASSEMBLY RELIABILITY

Thermal impact :

With conventional mounting (face-up mounted) a maximum junction temperature of 148°C is obtained with a case temperature of 55°C and biasing condition giving about 90 mW per finger. This result was compared to different flip-chip configurations. The results of the electrothermal calculations using various bump and substrate configurations are shown in Fig.4.

With the optimized configuration (centered bump version with 3 µm metal coating on AlN or shifted bump version with 22 µm metal coating) we found a maximum junction temperature of 115°C, which is indeed 30 °C lower as compared with conventional face up-mounted devices. This put forward the potential of the flip-chip mounting technology for high power density components such as HBT.

	Conventional mounting	Flip-Chip mounting offset bar (5µm) AlN metal thickness 3 µm	Flip-Chip mounting centered bar AlN metal thickness 3 µm	Flip-Chip mounting offset bar (5µm) AlN metal thickness 22 µm
$\overline{Rth\ moy}$	103,3 °C/W	67 °C/W	59 °C/W	61,6 °C/W
Improvement of $\overline{RTH\ moy}$	0	35%	43%	40%
$\overline{T\ moy}$	130 °C	103 °C	98 °C	100 °C
Improvement of $\overline{T\ moy}$	0	21%	25%	23%
Rth max central fingers	1080 °C/W	757 °C/W	645 °C/W	716 °C/W
Improvement of Rth max	0	30%	40%	34%
T max central fingers	148 °C	125 °C	115 °C	121 °C
Improvement of T max	0	16%	22%	18%

Fig.4 : electrothermal calculation of FC mounted 8 fingers HBT into various configurations compared to standard face-up mounted devices (Bias point Vce = 9 V, Ib = 1,76 mA, Pd = 722mW, case temperature : Tc = 55 °C)

These models have been validated using electrical method to measure the Rth drop from conventional face-up mounted devices when compared. Using the Vbe turn-on voltage drift method, we confirmed a Rth decrease of about 30 % when the HBT is flip-chip mounted (shifted bump version) on 3µm thick gold coated AlN substrate. Measured data on 6 fingers HBT, in shifted bump version, flip-chip mounted on AlN carrier has exhibited 145 °C/W at Tj=100 °C with a confirmed dVbe/dt=1.4 mV/°C. For a similar device, face-up mounted to a CuW carrier, we obtained 205 °C/W at Tj=100 °C.

Assembly reliability :

Flip-chip assembly was done on AlN substrate using the thermocompression process parameters validated within the frame of this project [5]. Three flip-chip mounted GaAs interconnect test chips over a total lot of 6 have been underfilled with commercial epoxy resin. They were all subsequently placed into a computer controlled oven for thermal cycling compliant with MIL STD 883 (55°C / 125°C). Electrical test using 4 probes

measurements were performed at initial, 100 cycles up to 1000 cycles with steps of 100 cycles. For the die flip-chip mounted with no underfill, failure occurred after 100 cycles for bumps located close-by the corner of the die. It then confirms that underfill is needed for large area die (5x5 mm^2).

Fig.5 shows the electrical test results of each daisy chains located at the corner of the test die (subject to the strongest displacement with temperature variation). Results for 3 flip-chip mounted interconnect test die with underfill are plotted. Note that bump contact resistance variation does not exceed 1 % up to 1000 cycles, except for one bump where the variation is about 10 %. Note that up to 200 thermal cycles are needed to qualify new assembly process for standard space product.

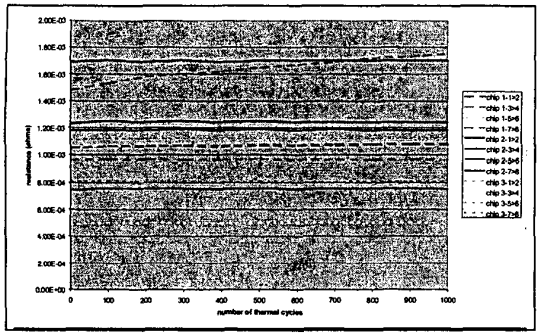

Fig.5 : Resistance variation of bump interconnect as a function of number of thermal shocks (-55°C, 125 °C). The GaAs test die was FC mounted on AlN with underfill.

Electrical impact :

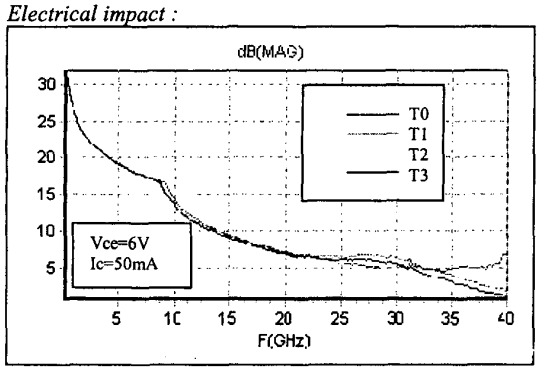

Fig.6 : S-parameters measurements, on wafer (T0), after flip-chip (T1), after underfill (T2), after 100 thermal shock (-55°C, +125°C) (T3)

In order to assess on possible degradation on HBT intrinsic characteristics due to the load applied during the assembly process or on extrinsic characteristics due to the surface proximity effect of the AlN substrate, S-parameter measurements were conducted on unmatched HBT cells up to 40 GHz. Fig.6 shows the gain curves of 6 fingers HBT in the following configurations : on wafer, after flip chip onto AlN and after underfill. The transistors showed a nearly identical behavior before and after flip-chip mounting & underfill. This is the result of the technology study reported elsewhere, showing that the thermal bump needs to be shifted from the emitter finger to limit the process induced stress.

IV. POWER PERFORMANCES

Impact of packaging

In order to assess on packaging impact, the HPA has been characterized on wafer in linear and non linear operating modes. On wafer power measurements were also performed using pulse test bench, to have a measured reference that could help assess on the insertion losses introduced by flip-chip mounting. Comparison was made for the same die before and after assembly : at 11.7 GHz in pulsed mode we measured 32 dBm output power at 2 dB gain compression with associated gain of 20dB, a power added efficiency of 25% for biasing condition of Vce=8V and Ic=490mA.

CW measurements for HPA module are plotted in Fig.7, showing more than 31 dBm of output power for the band 11-12 GHz. If we compare the measured output power of 31.3 dBm obtained in CW mode at 11.5 GHz, with what could be measured in pulse mode, one can say that the 0.7 dB insertion loss is not linked to the flip-chip mounting process but due to both the CPW to microstrip and microtrip to coax transitions (respectively 2x0.1 dB and 2x0.2 dB measured at 12GHz).

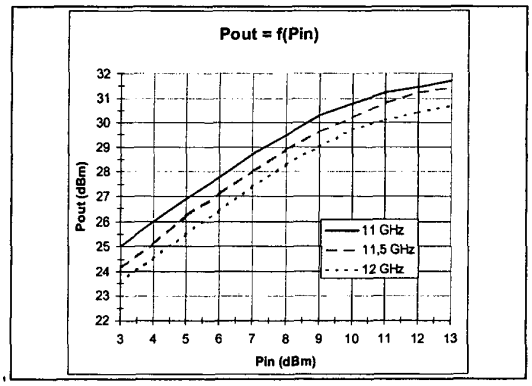

Fig.7 : Pin vs Pout curves in Ku band of a fully packaged HPA

Overall CW performances of the HPA with improved thermal management (power flip-chip) were comparable to the measurements made on-wafer in pulse mode. In Fig.7 we measured at 11.5 GHz, Pin=12dBm, P2dB= 31.3dBm, Gain=21.3dB, PAE=22% with biasing conditions Vce=8V and Ic= 505 mA.

Impact of underfill

Due to CTE mismatch between GaAs and AlN, it has been shown in the previous section that underfilling between the GaAs die and the host substrate was needed to be compliant with space applications.

Fig.8 is showing small signal gain curves before and after underfill. In linear regime, we see that the gain remains unaffected by the underfilling, a frequency shift in the lower frequencies of about 200 MHz has to be reported.

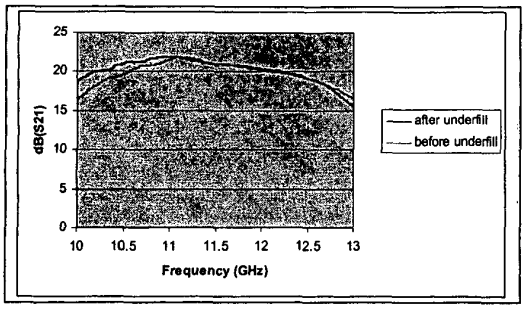

Fig.8 : Impact of underfill resin on linear gain curves

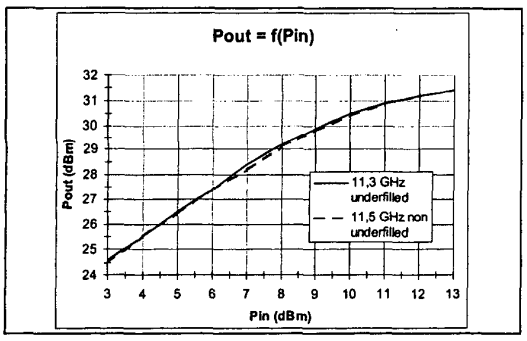

Fig.9 : Impact of underfill resin (FP 4511 from Dexter) on Pin vs Pout curves

Using the results obtained on the small signal gain curves frequency shift we have performed Pin vs Pout power measurement before underfill at 11.5 GHz and after underfill with a frequency shift of 200 MHz (11.3 GHz).

The results presented in Fig.9 shows that the two Pin vs Pout curves matches, showing that the underfill resin is not degrading the intrinsic characteristics of the die. It shows also that a design could be done to correct for this frequency shift to account for this dielectric constant change (from air to epoxy resine (K=3.5)).

V. Conclusion

In this paper, we have demonstrated operation of flip-chip mounted, HBT based, HPA MMIC in Ku band compliant with space environment constraints. In more details, up to 32 dBm output power was measured in CW mode at 11 GHz with 20 dB gain and 22 % PAE. Minimum losses introduced by the packaging compared to on-wafer measurements has been measured.. Further results on DC and dynamic reliablity of this power module will be available at the time of the conference.

In addition, one has to put forward that junction temperature remains very low thanks to the thermal bumps allowing 30 % Rth drop compared to face-up mounted devices .

ACknowledgement

The authors would like to acknowledge the European Commission for funding into the ESPRIT framework under contract APOS (Advanced high power subassemblies) reference #28270.

References

[1] D. Hill, T. S. Kim "28 V Low thermal Impedance HBT with 20 W CW Output power", *IEEE Transactions on microwave theory and techniques*, pp. 2224-2228, vol. 45, N°12, Dec 97.

[2] S. Keller, et al. ," Gallium nitride based high power heterojunction field effect transistors: Process development and present status at UCSB", *IEEE Transactions on microwave theory and techniques*, pp. 552-559, VOL. 48, NO. 3, MARCH 2001

[3] M. Schlechtweg et al ,"Coplanar MMICs up to 100GHz for communication and sensor systems", *APMC'99*, Workshop1, November 1999.

[4] A. Bessemoulin, et al, "Design of coplanar power amplifiers for mm-wave system applications including thermal aspects", *GAAS 2000*, pp224-227, October 2000.

[5] O. Vendier, et al., "Power flip-chip assembly for space applications using HBT in Ku band" *22nd GaAs IC Symposium*, pp157-159, November 2000.